IN THE CLAIMS

Please amend claims 14 and 25 to address informalities. No other amendments are being made.

1. (Original) A method of estimating a critical path delay during a source electronic design placement into a target hardware device, comprising:

receiving an electronic representation of the source electronic design;

determining a path criticality in the source electronic design based on,

determining an actual delay corresponding to a connection already placed across a first boundary in the target device, and

determining a statistical estimate for a future delay corresponding to an associated future connection to be placed across a second boundary in the target device; and

partitioning at least a portion of the source design by placing at least the portion of the source design across boundaries in the target device based on the determined actual delay and the statistical estimate for a future delay.

2. (Original) The method of claim 1 wherein the placing is biased towards a state in which an individual path having a relatively high criticality is not changed so as to increase an associated delay.

3. (Original) The method of claim 1 wherein the placing is biased towards a state in which an individual path having a relatively high criticality is changed in a manner that reduces the associated delay.

4. (Original) The method of claim 2 wherein the estimate for the future delay is generated by performing partitioning techniques on at least one other electronic source design.

5. (Original) The method of claim 1 wherein the electronic representation is received in the form of hardware description language coding.

6. (Original) The method of claim 1 wherein the electronic representation is received in the form of a schematic electronically captured.

7. (Original) The method of claim 1 wherein the electronic representation is received in the form selected from a group comprising: a netlist, an electronically captured schematic, and a coded hardware description language.

8. (Original) The method of claim 1 wherein the connections include at least one of conductive lines and switches.

9. (Original) The method of claim 1 wherein the target hardware device is selected from a group comprising: a complex programmable logic device (CPLD), a field programmable gate array (FPGA), an application specific integrated circuit (ASIC), a programmable logic device, a general purpose microprocessor, and a board level circuit implementation.

10. (Original) The method of claim 1 further comprising iteratively repeating the determining a path criticality and the partitioning at least a portion of the source design.

11. (Original) The method of claim 1, further comprising:

determining whether to repartition the at least a portion of the source design after the partitioning; and

if necessary, adjusting the estimates of delays from future partitions.

12. (Original) The method of claim 11 wherein determining whether to repartition at least a portion of the source electronic design is determined by comparing the critical path delays resulting from the partitioning cut with the estimate of critical path delays prior to the partitioning cut.

13. (Original) The method of claim 10 wherein adjusting the estimates of delays from future partitions comprises:

substituting a percentage of delays attributed to the partition in the statistical estimate with a new percentage derived from the critical path delay results from the partition.

14. (Currently Amended) The method of claim 1 wherein the statistical estimate for future delay comprises:

receiving at least one source design;

placing the at least one source design using partitioning methods to place the device

across boundaries in the target device; and

generating statistical data corresponding to each type of boundary crossed in the target device.

~~wherein the statistical data represents the proportion of each hierarchical type of cut of the entire number of cuts in the fully placed design~~

15. (Original) The method of claim 14 wherein the statistical data represents the proportion of each hierarchical type of cut of the entire number of cuts in the fully placed design.

16. (Original) The method of claim 15 wherein the statistical estimates correspond to the weighted average of the statistical data generated.

17. (Original) The method of claim 16 wherein the weighted average is based on a predetermined number or percentage of the slowest delays.

18. (Original) The method of claim 16 wherein the weighted average is based on a predetermined number or percentage of the fastest delays.

19. (Original) A method for generating statistical estimates for future delays on uncut connections on a path in placing a design by partitioning methods comprising:

receiving at least one source design;

placing the at least one source design using partitioning methods to place the device across boundaries in the target device; and

generating statistical data corresponding to each type of boundary crossed in the target device.

20. (Original) The method of claim 19 wherein the statistical data represents the proportion of each hierarchical type of cut of the entire number of cuts in the fully placed design.

21. (Original) The method of claim 19 wherein the statistical estimates correspond to the weighted average of the statistical data generated.

22. (Original) The method of claim 21 wherein the weighted average is based on a predetermined number or percentage of the slowest delays.

23. (Original) The method of claim 21 wherein the weighted average is based on a predetermined number or percentage of the fastest delays.

24. (Original) A computer program product comprising:

a machine readable memory on which is provided program instructions for a method of placing a source electronic design into a target hardware device by partitioning methods, the instructions comprising:

code for receiving an electronic representation of the source electronic design;

code for determining a path criticality in the source electronic design based on determining an actual delay corresponding to a connection already placed across a first boundary in the target device,

code for determining a statistical estimate for a future delay corresponding to an associated future connection to be placed across a second boundary in the target device; and

code for partitioning at least a portion of the source design by placing the at least a portion of the source design across boundaries in the target device based on the criticalities determined.

25. (Currently Amended) The computer program product of claim 24 wherein the code for determining the statistical estimate for future delay comprises:

code for receiving at least one source design;

code for placing the at least one source design using partitioning methods to place the device across boundaries in the target device; and

code for generating statistical data corresponding to each type of boundary crossed in the target device,

~~wherein the statistical data represents the proportion of each hierarchical type of cut of the entire number of cuts in the fully placed design~~

26. (Original) The computer program product of claim 25 wherein the statistical data represents the proportion of each hierarchical type of cut of the entire number of cuts in the fully placed design.

27. (Original) The computer program product of claim 26 wherein the statistical estimates correspond to the weighted average of the statistical data generated.

28. (Original) The computer program product of claim 27 wherein the weighted average is based on a predetermined number or percentage of the slowest delays.

29. (Original) The computer program product of claim 28 wherein the weighted average is based on a predetermined number or percentage of the fastest delays.

30. (Original) A computer system having a central processing unit (CPU) coupled to a memory, comprising:

an interface for communicating with an individual;

wherein the computer system is configured to receive an electronic representation of the source electronic design;

wherein the computer system is further configured to,

determine a path criticality in the source electronic design based on determining an actual delay corresponding to a connection already placed across a first boundary in the target device, and

determine a statistical estimate for a future delay corresponding to an associated future connection to be placed across a second boundary in the target device; and

wherein the computer system is further configured to partition at least a portion of the source design by placing the at least a portion of the source design across boundaries in the target device based on the determined actual delay.